electrode is also in electrical contact with the channel layer. A gate is included also in electrical contact with the channel layer between the source and drain electrodes. A spacer layer is on at least part of the surface of the channel layer between the gate and the drain electrode and between the gate and the source electrode. A field plate is on the spacer layer, extending on the spacer over the channel layer toward the drain electrode and extending on the spacer layer over the channel layer toward the source electrode. At least one conductive path electrically connects the field plate to the source electrode or the gate.

[0012] These and other further features and advantages of the invention would be apparent to those skilled in the art from the following detailed description, taken together with the accompanying drawings, in which:

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] **FIG. 1** is a plan view of one embodiment of a HEMT according to the present invention;

[0014] **FIG. 2** is a sectional view of the HEMT shown in **FIG. 1**;

[0015] **FIG. 3** is a sectional view of another embodiment of a HEMT according to the present invention;

[0016] **FIG. 4** is a sectional view of another embodiment of a HEMT according to the present invention;

[0017] **FIG. 5** is a sectional view of another embodiment of a HEMT according to the present invention having multiple field plates;

[0018] **FIG. 6** is a sectional view of another embodiment of a HEMT according to the present invention having multiple field plates;

[0019] **FIG. 7** is a sectional view of another embodiment of a HEMT according to the present invention having multiple field plates;

[0020] **FIG. 8** is a sectional view of another embodiment of a HEMT according to the present invention;

[0021] **FIG. 9** is a sectional view of one embodiment of a MESFET according to the present invention;

[0022] **FIG. 10** is a sectional view of another embodiment of a MESFET according to the present invention; and

[0023] **FIG. 11** is a table comparing the operating characteristics of a HEMT according to the present invention compared to a HEMT with no field gate-source field plate.

DETAILED DESCRIPTION OF THE INVENTION

[0024] The gate-source field plate arrangements according to the present invention can be used with many different transistor structures, such as transistor structures made of wide bandgap materials. Transistors generally include an active region having a plurality of semiconductor layers, one of which is a channel layer. Metal source and drain electrodes formed in contact with the active region, and a gate formed on the active region between the source and drain electrodes for modulating electric fields within the active region. A first spacer layer is formed above the active region, over at least a portion of the surface of the active region between the gate and the drain. The first spacer layer can comprise a dielectric layer or a combination of multiple dielectric layers, and in certain embodiments other materials such as epitaxially grown layers. In one embodiment the first spacer layer covers the gate and the topmost surface of the active region between the gate and the drain electrode, and between the gate and the source electrode. In other embodiments as described below the spacer layer can cover less of the surface of the active region. In still other embodiments the spacer layer covers only the topmost surface of the active region between the gate and the source and drain, and not the gate.

[0025] A conductive first field plate is formed on the first spacer layer with the first spacer layer providing isolation between the field plate the active region below. The first field plate extends a distance L_{fd} on the spacer layer from the edge of the gate toward the drain electrode, and extends a distance L_{fs} on the spacer layer toward the source electrode. The first field plate can be electrically connected to either the source electrode or the gate. Additional spacer layer field and field plate pairs can also be included in different embodiments according to the invention.

[0026] This field plate arrangement can reduce the peak electric field in the device on both the source and drain side of the gate, resulting in increased breakdown voltage and reduced trapping. The reduction of the electric field can also yield other benefits such as reduced leakage currents and enhanced reliability. The field plates on both the source and drain sides of the gate are arranged such that the electric field on the source side of the gate is reduced, which enhances performance and robustness for applications that require more negatively biased gate conditions. This includes class-C and other higher classes (e.g. E, F) of operations. By having the field plate on the drain side as well, the transistor also experiences reduced peak electric field on the drain side.

[0027] One type of transistor that can utilize the gate-source plate arrangement according to the present invention is a high electron mobility transistor (HEMT), which typically includes a buffer layer and a barrier layer on the buffer layer. A two dimensional electron gas (2DEG) channel layer is induced at the heterointerface between the buffer layer and the barrier layer. A gate electrode is formed on the barrier layer between source and drain electrodes. The HEMT also includes the multiple spacer layer and field plate arrangement described above.

[0028] Another type of transistor that can utilize the gate-source field plate arrangement according to the present invention is a field effect transistor and particularly a metal semiconductor field effect transistor (MESFET), which typically includes a buffer layer and a channel layer on the buffer layer. A gate is formed on the channel layer between source and drain electrodes and the MESFET also includes the multiple spacer layer and field plate arrangement described above.

[0029] It will be understood that when an element or layer is referred to as being "on", "connected to", "coupled to" or "in contact with" another element or layer, it can be directly on, connected or coupled to, or in contact with the other element or layer or intervening elements or layers may be present. In contrast, when an element is referred to as being "directly on,""directly connected to", "directly coupled to" or "directly in contact with" another element or layer, there